ABSTRACT

An error detector for a pseudo-random bit sequence (PRBS). A plurality of bits of a PRBS are received in a predictor circuit. A comparator compares two of the bits to predict a next bit in the sequence. The predicted next bit is compared with the actual next bit that is received to determine if there is an error in the actual next bit, and if so, the actual next bit is corrected accordingly. The erroneous actual next bit is replaced with the corrected actual next bit and is then used to predict a future actual next bit. A trigger circuit delays correction during initial operation until the predictor contains a bit sequence in which no errors have been detected.